横川慎二　研究室

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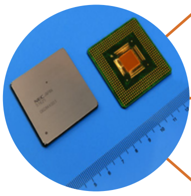
研究テーマ②：半導体デバイスの超長期信頼性に関する研究



メモリデバイス
- 超長期データ保存
- 低消費電力

- ✓ Electromigration, Stress-induced Voiding, Low-k TDDBなどの磨耗故障抑制のためのプロセス技術・評価の研究
- ✓ 超長期信頼性保証のための故障メカニズムの調査研究

パワーデバイス
- 高速動作
- 新規デバイス導入

- ✓ GaN, SiCデバイスの故障メカニズムに関する調査研究

ロジックデバイス
- 高信頼性
- 高品質（初期故障抑制）

- ✓ 非一様性（欠陥クラスタリング）を仮定した大規模Segmentデバイスの寿命分布に関する研究
- ✓ 故障メカニズムに基づく高信頼設計技法の研究

Void growth＝Stress-induced Cu transportation

① Relation between void volume and atomic transportation

$$\frac{dV_v(t)}{dt} = J(t)\Omega \quad (1)$$

Change in void volume
＝Atomic flux ×
Atomic volume

② Okabayashi's atomic transportation model (1993)

$$J(t) = A\frac{GD_{\mathrm{eff}}}{kT}\left[\frac{\sigma(t)}{G}\right]^n \quad (2)$$

Atomic flux
＝Mobility ×
Driving force

Relation between stress and void volume

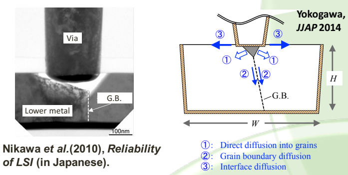
$$\sigma(t) = \frac{1}{3}\left[\sigma_x(t)+\sigma_y(t)+\sigma_z(t)\right]$$

$$\approx \sigma(0) - \frac{EV_v(t)}{3(1-2\nu)V_{\mathrm{ASRV}}} \quad (3)$$

1) Stress = Initial stress – Relaxation by void growth
2) Stress relaxation has a term in inverse proportion to Active Stress Relaxation Volume (ASRV)

bulk, grain boundaries, top interface, and liner interface

$$D_{\mathrm{eff}} \approx D_b + \frac{\delta_{gb}}{L_d\cdot\cos\theta_1\cdot\cos\theta_2}\cdot D_{gb} + \frac{\delta_s}{H}\cdot D_s + \delta_i\left(\frac{1}{H}+\frac{2}{L_d}\right)\cdot D_i \quad (4)$$



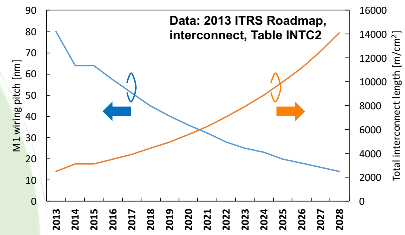
Nikawa et al.(2010), Reliability of LSI (in Japanese).

Time-dependent change in void volume is lead from eqns. (1), (2), and (3).

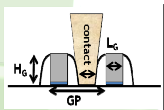
$$\frac{dV_v(t)}{dt} = \frac{AG\Omega}{kT}D_{\mathrm{eff}}\left[\frac{\sigma(0)}{G} - \frac{E}{3(1-2\nu)}\frac{V_v(t)}{GV_{\mathrm{ASRV}}}\right]^n \quad (5)$$

Lifetime can be derived for a threshold of void volume that causes the open failure.

$$\tau = \frac{3(1-2\nu)V_{\mathrm{ASRV}}kT}{(n-1)AE\Omega D_{\mathrm{eff}}}\left[\left(\frac{G}{\sigma(\tau)}\right)^{n-1} - \left(\frac{G}{\sigma(0)}\right)^{n-1}\right] \quad (6)$$



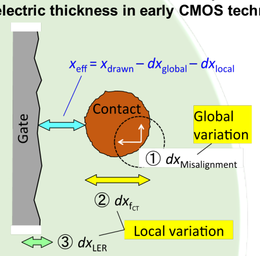
J.H. Stathis, et al., IEDM 2014

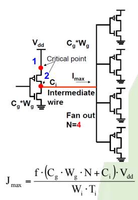


Node	Gate Pitch	Gate Length	Contact	Best case Spacer
32	120-130	30-35	30-40	25-30
22-14	80-100	25-30	20	18-25
10	65-75	20-23	20	12-16
7	45-55	12-18	15	9-12
5	35-45	9-16	12	7-9
3?	25-35	7-12	<12?	3-6?

Best case spacer = (GP-L_G-Contact)/2

The spacing between the gate and the S/D contact will become less than 10nm which is comparable to the gate dielectric thickness in early CMOS technology.





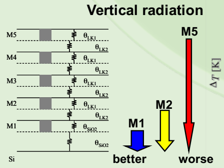
Critical point 1:
Pulsed direct current (PDC)
Javg > large　EM Issue
Jrms > large　JH Issue

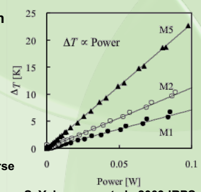
Critical point 2:
Pulsed alternate current (PAC)
Javg > small
Jrms > large　JH Issue

✓Improvement of EM
✓JH management
✓EM under PDC/PAC with JH

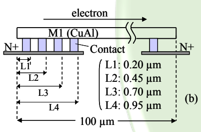
$$J_{max} = \frac{f\cdot(C_g\cdot W_g\cdot N + C_i)\cdot V_{dd}}{W_i\cdot T_i}$$

Vertical radiation

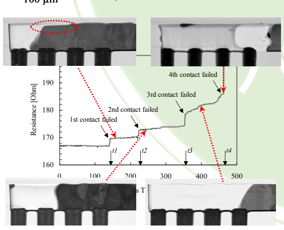


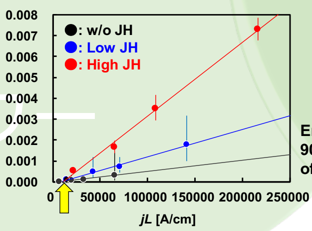


S. Yokogawa, et al., 2009 IRPS



Drift structure*):
•Drift velocity of Cu (W=120 nm)
•Incubation time until void nucleation
*) Kawasaki and Hu (1996)





Error bar:
90% C.L.
of estimates

1. **Weibull distribution**

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^\beta\right]$$

2. **Clustering model for lifetime distribution**

$$F(t) = 1 - \left\{1 + \frac{D}{\alpha}\left(\frac{t}{\eta}\right)^\beta\right\}^{-\alpha}$$

$\alpha\to\infty$: Weibull distribution
$D\to 1$: Wu, et al., APL (2013)